LeCroy

MEMORY MODULE
MODEL 8800A

Revised
April, 1984

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ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily answered by a member of our Engineering Services Department, telephone 914-425-2000 or your local distributor. You may address any correspondence to:

LeCroy Research Systems Corp., 700 S. Main Street,
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A T T E N T I O N

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID DAMAGE CAUSED BY MOMEMTARY MISALIGNMENT OF CONTACTS.

A T T E N T I O N

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TECHNICAL DATA

LeCroy

CAMAC Model 8800A
Memory Module

The Model 8800A is designed to provide data storage for a wide variety of LeCroy instruments, including transient recorders, video digitizers, and fast data loggers. Each module has a capacity for 32K 12-bit data words and modules may be cascaded to provide record lengths to 256K words.

All read and write operations to the 8800A are controlled by the companion digitizer. Data from the digitizer is sequentially stored as acquired; if the controlling unit has more than one channel, the total of all cascaded memory is divided equally among the active channels. During readout to the CAMAC dataway, the memory contents are reconstructed so that each channel's data is in contiguous time sequence.

Readout is nondestructive and the memory is protected against write operations from the CAMAC dataway; it can only be written from the companion digitizer.

The Model 8800A Memory module is compatible with the following LeCroy digitizers:

Model 2264	8 channel, 0.5 MHz 8-bit Waveform Digitizer
Model 8210	4 channel, 1 MHz 10-bit Waveform Digitizer
Model 8212A	32 channel, 0.5-40 kHz, 12-bit Data Logger
Model 8212A/8	8 channel, 12.5-100 kHz, 12-bit Data Logger

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Innovators in Instrumentation

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TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
CAMAC Model 8800A
MEMORY MODULE

Inputs:

TTL Levels. Lines: 12 data, 12 grounds; 7 control lines, 7 grounds. One 40-conductor edge connector located at the upper rear of the module. Mates with LeCroy Model DC8800/n Data Cable (where "n" equals the number of memory modules linked to one data acquisition device.

Memory Active Light:

Front-panel LED indicates when memory is being loaded or read.

Memory Size:

32,768 words, 12 bits.

Memory Expansion:

Serial organization permits adding the Model 8800A modules in a daisy-chained fashion with the maximum memory size dictated by the control board of the ADC module. Memory size must be internally specified on the control board of the "front end" ADC (jumper option) and on the memory modules (onboard Programming Switch). The LeCroy Models 2264 and 8210 can drive three modules, and Model 8212A can drive four modules with larger memory extention possible as a factory option.

Packaging:

In conformance with the international CAMAC standard for nuclear modules (European ESONE Report #EUR4100 or U.S. IEEE Report #583). RF-shielded CAMAC #1 module.

Power Supplies:

The Model 8800A Series can draw + 12 V from the + 12 V CAMAC bus or can be jumpered internally to use a built-in + 24 to + 12 V converter. Since the memory is not read directly, it can be located in an adjacent power crate (<4 feet of cable) with only + 12, + 6 V power.

Power Consumption:

Voltage	Current	Power
+ 12 V (or + 24 V)	490 mA	5.9 W (11.8 W)
+ 6 V	650 mA	3.9 W
− 6 V	30 mA	0.2 W

Total Power Dissipated:

10 W (+ 12 V), 15.9 W (+ 24 V)

SPECIFICATIONS SUBJECT TO CHANGE

SECTION 2

2. OPERATING INSTRUCTIONS

2.1 General

The LeCroy 8800A module is a dynamic memory with a capacity of 32,768 12-bit words. It is designed especially for high speed (up to 5 megawords/sec) sequential storage of data. The input data is multiplexed into two banks of 16K dynamic RAM memory and is then written into the memories in a page mode memory cycle as the memories are addressed by on board counters. During readout the data is multiplexed onto the I/O lines from the two memory banks in the same order that it was written into the memory. The entire memory (per digitizer channel) must be read out to reach the last word written.

Since these units are dynamic RAM's the 128 rows in the memory banks must all be addressed at least once every 2 msec. When memory cycles occur at a rate too low to satisfy this condition, refresh cycles must be inserted by appropriately timed refresh pulses on the Model 8800A refresh control line. Multiplexing of the data into the memory and memory address increment are controlled by memory clock pulses on the memory strobe line. Read or write operation is determined by the logic level on the read/write control line. The logic circuits are reset or initialized by a TTL low pulse on the initialize line. In addition, these units are designed so that they may be cascaded to increase memory size. To facilitate this mode of operation, each module has two memory enable lines and a memory enable return line. All of the above mentioned control lines as well as the I/O lines for the data are accessed via a rear panel 40 pin header.

2.2 Front Panel Indicator

An LED lamp lights when memory module is enabled for read or write operations. When cascaded memory modules are being used, this allows the user to see which module is currently receiving or dispensing data.

2.3 Rear Edge-Connector Signals (see Pin Assignments diagram, Figure 2.1)

INITIATE: Minimum 400 nsec pulse to initialize memory address registers to zero and reset internal logic.

MEM1: TTL low, indicates the module has been completely written or read. This signal is used to enable the next even 8800A to read or write data. Maximum signal duration should be between 100 and 150 nsec.

MEM2:	Same as MEM1, except used to enable the next odd 8800A to read or write data.
MEM RTN:	Same as MEM EN lines except this signal is transmitted back to the digitizer module's controller. MEM EN RTN is generated by the last memory module on the bus.
REFRESH:	TTL high pulse, minimum duration is 200 nsec. This signal initiates a refresh cycle in the memory module.
CLOCK:	TTL high pulse, minimum duration is 50 nsec. This signal stores data in the input latches during write operations. Alternate clock pulses initiate memory cycles. During readout the signal alternately enables bank #1 and #2 output latches (see functional description, Section 3) and alternate clock pulses will initiate memory cycles.
R/W:	TTL high to write, low to read. Transition from high to low initiates memory cycle which locks data into output latches.
DATA LINES (2^{11}-2^{0}):	Bidirectional TTL data, 2^{11} is the MSB and 2^{0} is the LSB.

2.4 Switch Settings (Refer to memory cabling and switch diagram, Figure 2.2)

Seven switches in a DIP package are accessible through a window in the side cover of the 8800A. Five of the switches are used to program the module for a position in a chain of modules, i.e., the switch positions will determine whether the module is to function in a first, last or intermediate position in the chain. The remaining two switches program the scanning of the memory addresses to be either by row or by column.

General Rules - A memory module may receive or generate memory enable pulses on either MEM1 or MEM2, but may not receive and generate on the same line; thus switches S1 and S6 or S2 and S7 should never be on simultaneously. The memory may either be scanned by row or column* thus switches 3 and 4 should always be in opposite states. A memory system may consist of a series of memory modules. The last module in the series must send a memory enable return (MEM RTN) pulse to the controller signalling the end of a memory scan or the beginning of a new memory scan, therefore switch 5 must be on only in the last module in the series.

Specific Example - The following example system will illustrate the use of the memory enable lines and detailed switch settings. If a chain of four memory modules are to be used to scan by row (i.e., each column element in a row is addressed before advancing to the next row), set switch 4 on and switch 3 off on all of the units.

Module #1 receives the enable pulse from the controller on MEM1, therefore, S2 must be on and S7 off. Module #1 must then send an enable pulse to Module #2 on MEM2, thus, S6 must be on and S1 off. To isolate the pulse on the MEM2 line from the controller, the MEM2 line between Module #1 and the controller must be cut.

Module #2 receives the enable pulse on MEM2, therefore S1 must be on and S6 off. Module #2 must now send an enable pulse to Module #3 on MEM1, thus S7 must be on and S2 off. To isolate this pulse on MEM1 from Module #1's MEM1 input, the MEM1 line between Module #1 and Module #2 must be cut.

Module #3 receives the enable pulse on MEM1, therefore S2 must be on and S7 off. The enable pulse to Module #4 must be sent on MEM2, thus S6 must be on and S1 off. To isolate this pulse from Module #2, the MEM2 line between Module #3 and Module #2 must be cut.

Module #4 receives the enable pulse MEM2, therefore S1 must be on and S6 off. Since Module #4 is the last in the chain it must send a memory enable return pulse back to the controller, thus S5 must be on (S5 on the first three modules must be off). S2 and S7 could both be turned off to disconnect MEM1 between Module #3 and Module #4, but it is recommended that MEM1 be cut between these modules.

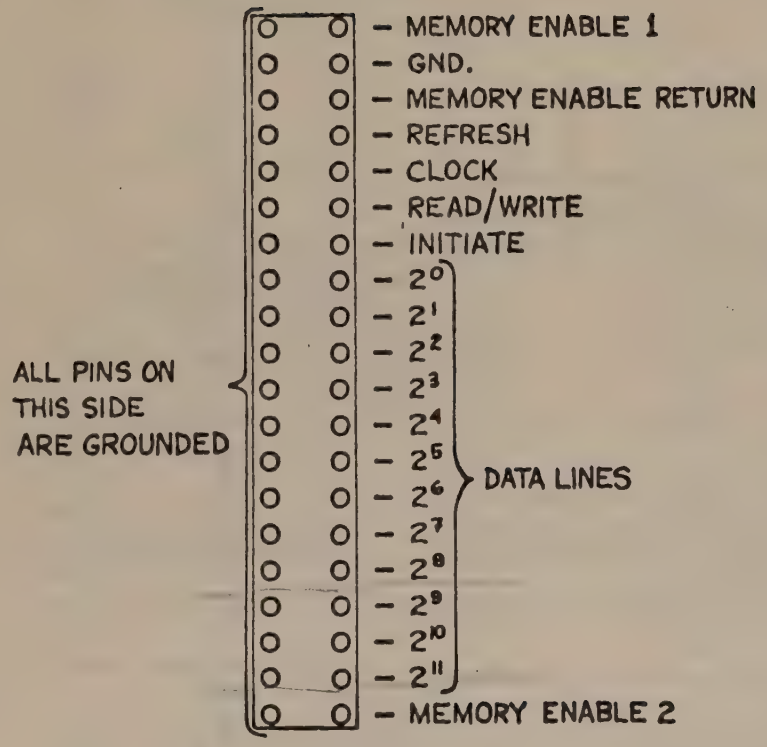
The MEM1 and MEM2 lines are the outside (upper and lower) control lines facilitating the necessary alternating cuts in these lines between units on the system.

* Scanning by column also requires an internal jumper connection (AG, pin 10).

2.5 Power

Since the 16K dynamic RAM's use +12 volts, an internal voltage regulator is supplied which will drop +24 volts to +12 volts. However, for CAMAC crates which supply power to their +12 V bus lines, the 8800A has internal jumpers (see schematic) allowing operation from +12 V which is in fact recommended due to lower total power dissipation.

The 8800A memory module uses no CAMAC control or data lines and may be placed in a dummy crate which contains power only. Consult factory concerning maximum bus cable lengths.


O O – MEMORY ENABLE 1
O O – GND.
O O – MEMORY ENABLE RETURN
O O – REFRESH
O O – CLOCK
O O – READ/WRITE
O O – INITIATE
O O – 2^0
O O – 2^1
O O – 2^2
O O – 2^3
O O – 2^4
O O – 2^5
O O – 2^6
O O – 2^7
O O – 2^8
O O – 2^9
O O – 2^{10}
O O – 2^{11}
O O – MEMORY ENABLE 2
ALL PINS ON THIS SIDE ARE GROUNDED
DATA LINES

PIN ASSIGNMENTS

for REAR CONNECTOR

(REAR VIEW SHOWN)

FIGURE 2.1

LeCROY RESEARCH SYSTEMS CORPORATION WEST NYACK, NEW YORK	
DRAWN S.MALM	MODEL 8800
CHECKED LGP	MEMORY MODULE
DATE 12/2/77	BLOCK DIAGRAM
DRAWING No. 8800/- RD1	SHT. 2 ECO No.

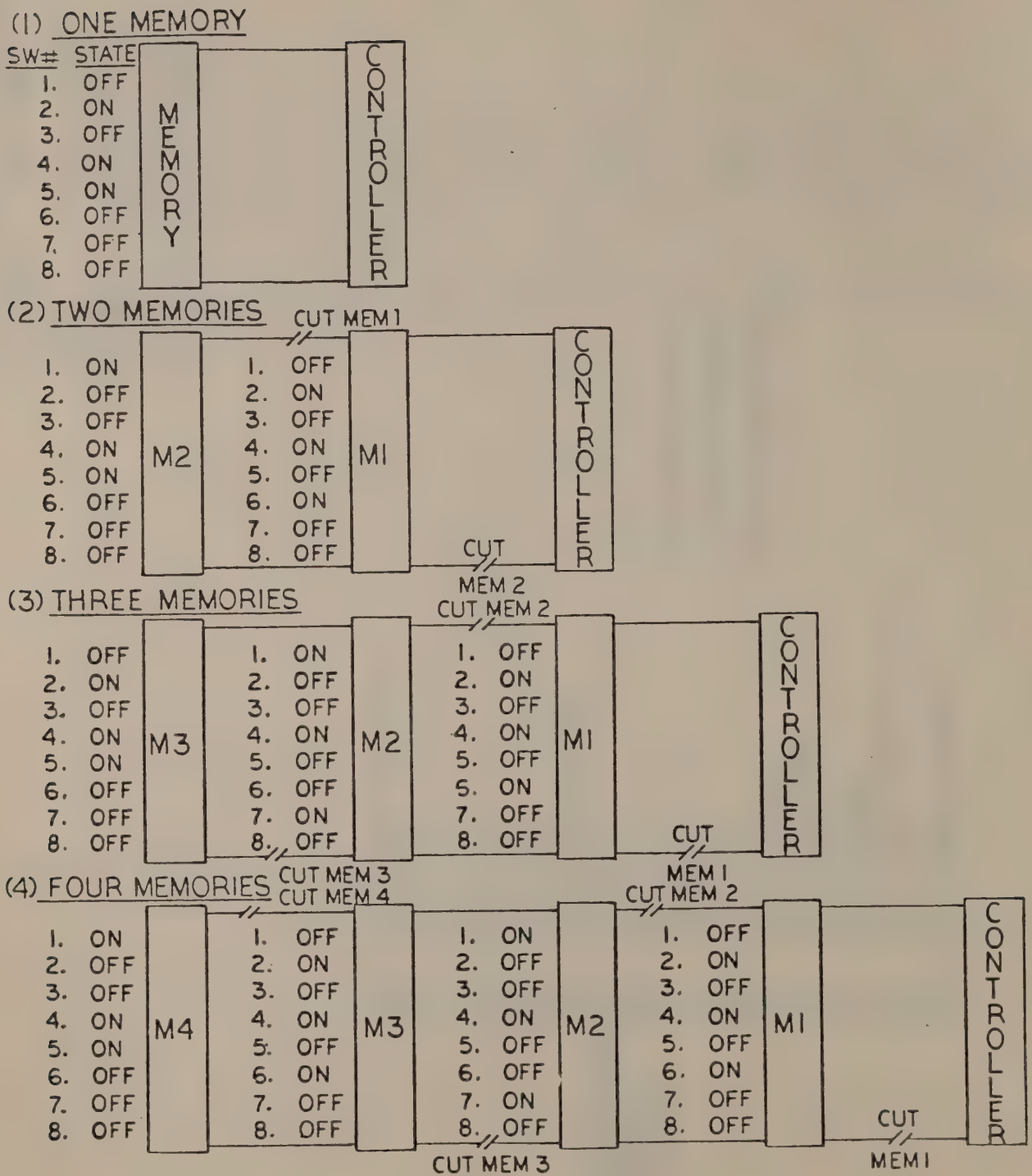

(1) ONE MEMORY
SW# STATE
1. OFF
2. ON
3. OFF
4. ON
5. ON
6. OFF
7. OFF
8. OFF
MEMORY
CONTROLLER
(2) TWO MEMORIES
CUT MEM 1
1. ON
2. OFF
3. OFF
4. ON
5. ON
6. OFF
7. OFF
8. OFF
M2
1. OFF
2. ON
3. OFF
4. ON
5. OFF
6. ON
7. OFF
8. OFF
M1
CUT
MEM 2
CONTROLLER
(3) THREE MEMORIES
CUT MEM 2
1. OFF
2. ON
3. OFF
4. ON
5. ON
6. OFF
7. OFF
8. OFF
M3
1. ON
2. OFF
3. OFF
4. ON
5. OFF
6. OFF
7. ON
8. OFF
M2
1. OFF
2. ON
3. OFF
4. ON
5. OFF
5. ON
7. OFF
8. OFF
M1
CUT
MEM 1
CONTROLLER
(4) FOUR MEMORIES
CUT MEM 3
CUT MEM 4
CUT MEM 2
1. ON
2. OFF
3. OFF
4. ON
5. ON
6. OFF
7. OFF
8. OFF
M4
1. OFF
2. ON
3. OFF
4. ON
5. OFF
6. ON
7. OFF
8. OFF
M3
1. ON
2. OFF
3. OFF
4. ON
5. OFF
6. OFF
7. ON
8. OFF
M2
1. OFF
2. ON
3. OFF
4. ON
5. OFF
6. ON
7. OFF
8. OFF
M1
CUT
MEM 1
CONTROLLER
CUT MEM 3

FIGURE 2.2

SECTION 3

3. FUNCTIONAL CIRCUIT DESCRIPTION

3.1 General

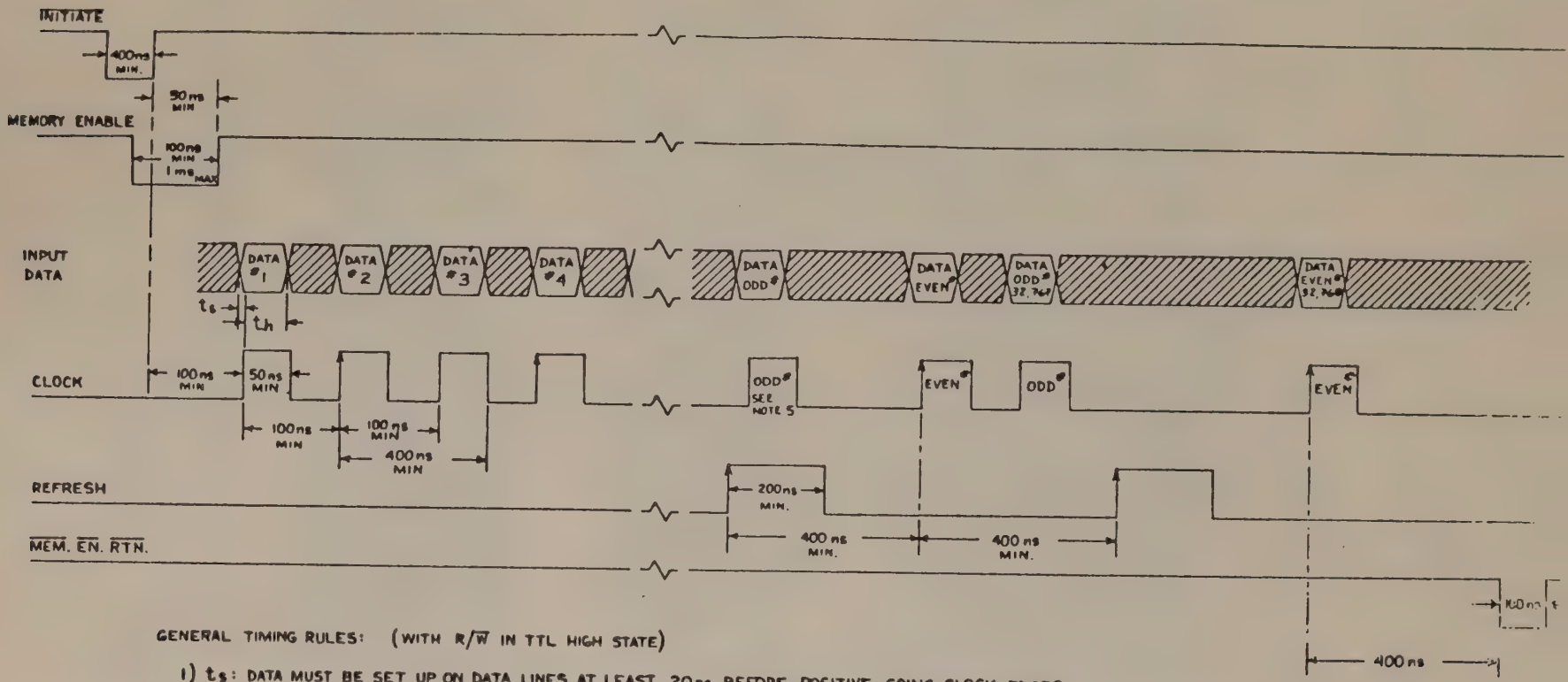
The LeCroy Model 8800A is a dual multiplexed memory consisting of 16K 12-bit words per memory bank (32K total). Write or read operations can be executed up to a 5 MHz average rate (see timing diagrams, Figures 3.1 and 3.2). The memory is only sequentially addressable when writing or reading. Since the 8800A uses 16K dynamic RAM's a minimum of 128 refresh pulses must be supplied every 2 msec. Refresh is accomplished by applying a 200 nsec (minimum) pulse to the refresh control line. The digitizer or memory controller module must generate this pulse at a time which ensures that memory read/write and refresh cycles do not overlap.

3.2 Writing Data

After the memory has been initialized and enabled (see Figure 3.1) data can be written into memory. The first clock pulse will strobe data into the input storage register for Memory Bank #1 (see block diagram, Figure 3.3). The second clock pulse will strobe data into Memory Bank #2, transfer Memory Bank #1 storage register data to the input latch and initiate a 400 nsec memory cycle which stores data. This sequence continues until the memory is filled and MEM RTN or MEM1/2 is generated. After this time the internal logic will disable the memory write pulse.

3.3 Reading Data

After the R/W control line changes state to a TTL low level, the 8800A will enter the readout mode (Figure 3.2). The R/W line transition initiates a memory readout cycle which loads data from the present memory address into Bank #1 and #2 output latches. At this time the input latches are disabled and Memory Bank #1's output latch is enabled onto the data bus. The first clock pulse will then disable Bank #1 output latch and enable Bank #2 output latch. The second clock pulse re-enables Bank #1 output latch, initiates a memory cycle and loads new data into the output latches. The sequence continues until the entire memory has been read out and MEM RTN or MEM1/2 is generated. After this time both output latches are disabled. (NOTE: During readout MEM RTN or MEM1/2 is generated immediately after the last two data words are stored in the output latches. The output latches will then automatically be disabled after the last two words have been readout).

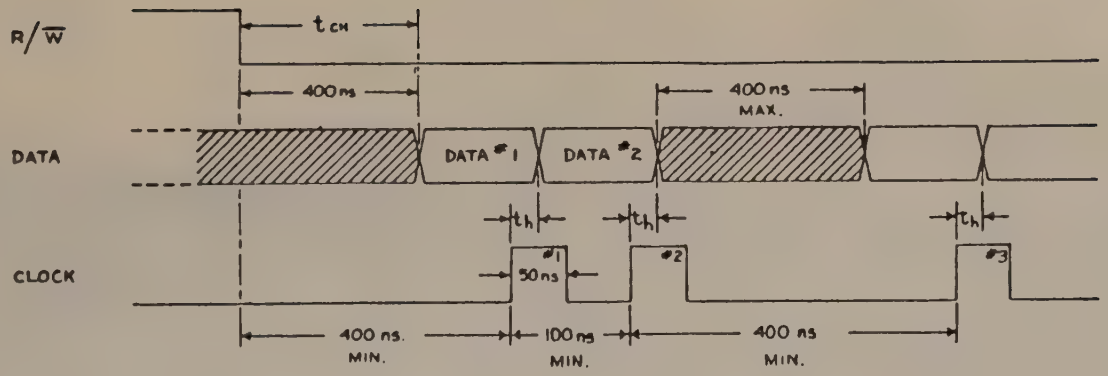


GENERAL TIMING RULES: (WITH R/$\overline{W}$ IN TTL HIGH STATE)

1) t_s: DATA MUST BE SET UP ON DATA LINES AT LEAST 20ns BEFORE POSITIVE GOING CLOCK EDGES.
2) t_h: DATA MAY CHANGE 50ns AFTER POSITIVE GOING CLOCK EDGES.
3) MEMORY CYCLES ARE INITIATED BY THE EVEN-NUMBERED CLOCK PULSES AND THE REFRESH PULSES (POSITIVE GOING EDGES, MARKED WITH ARROWS IN THE ABOVE DIAGRAM.) THESE EDGES MUST BE SEPARATED BY A MINIMUM MEMORY CYCLE TIME OF 400 ns. ODD-NUMBERED CLOCK PULSES ONLY STROBE DATA INTO MULTIPLEXING BUFFER REGISTERS.
4) REFRESH PULSES: MINIMUM 200ns DURATION (MINIMUM 128 PULSES EVERY 2 ms)
5) ONLY ODD-NUMBERED CLOCK PULSES MAY OCCUR DURING REFRESH.

LeCroy RESEARCH SYSTEMS		
S.MALM	MODEL 8800 TIMING DIAGRAM WRITE OPERATIONS	
1/23/78		
8800-TD1	SHEET 1 OF 2	ECO NO. DATE 10/6

FIGURE 3.1



GENERAL TIMING RULES: (WITH MEMORY WRITTEN INTO AS DESCRIBED IN 8800-TD1, SHEET 1)

1) t_{CH} : NO REFRESH OR CLOCK PULSES ARE ALLOWED DURING THIS TIME OR THE 400 ns PRECEDING THE R/W TRANSITION.
2) DATA #1 CORRESPONDS TO [LAST ODD DATA + 1] WRITTEN INTO MEMORY.
3) t_h: ~20ns
4) REFRESH TIMING AND CONDITIONS, MEM. EN. RTN. " " " } SAME AS DURING WRITE OPERATIONS.

FIGURE 3.2

LeCroy RESEARCH SYSTEMS		
S MALM	MODEL 8800	
CHECKED	TIMING DIAGRAM	
1/29/78	READ OPERATIONS	
8800 TD 1	SHEET 2 of 2	ECO NO DATE 10C

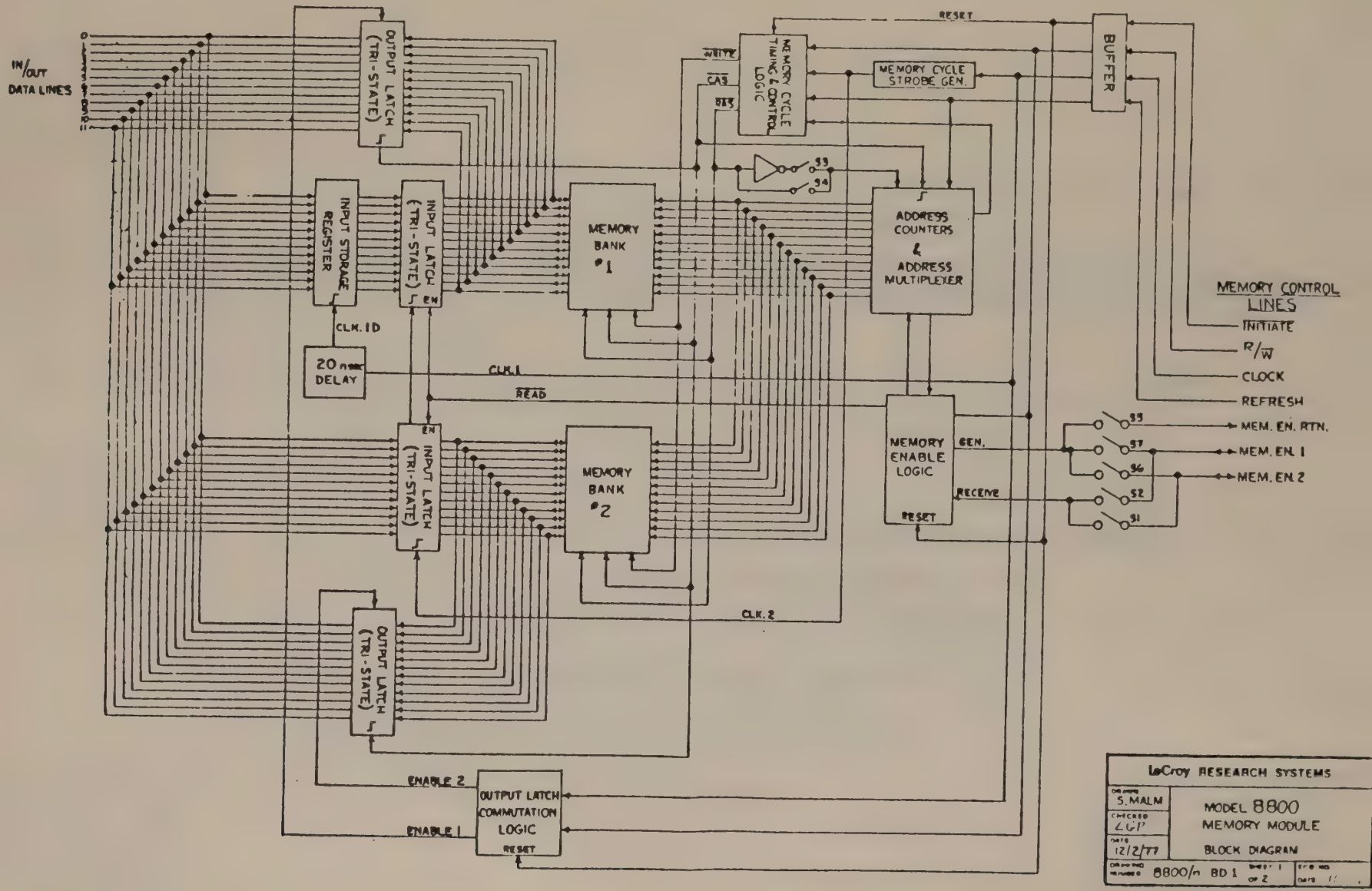

IN/OUT DATA LINES
OUTPUT LATCH (TRI-STATE)
INPUT STORAGE REGISTER
INPUT LATCH (TRI-STATE)
EN
CLK.1D
20 n DELAY
MEMORY BANK #1
MEMORY BANK #2
WRITE
CAS
RAS
MEMORY CYCLE TIMING & CONTROL LOGIC
MEMORY CYCLE STROBE GEN.
RESET
BUFFER
ADDRESS COUNTERS & ADDRESS MULTIPLEXER
S3
S4
CLK.1
READ
MEMORY ENABLE LOGIC
GEN.
RECEIVE
RESET
S5
S7
S6
S2
S1
CLK.2
ENABLE 2
ENABLE 1
OUTPUT LATCH COMMUTATION LOGIC
RESET
MEMORY CONTROL LINES
INITIATE
R/W
CLOCK
REFRESH
MEM. EN. RTN.
MEM. EN. 1
MEM. EN. 2
LeCroy RESEARCH SYSTEMS
S. MALM
LGP
12/2/77
MODEL 8800
MEMORY MODULE
BLOCK DIAGRAM
8800/n BD 1
SHEET 1 OF 2

FIGURE 3.3

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